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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,671	08/13/2001	Dennis M. O'Connor	INTL-0606-US (P11747)	8164

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EXAMINER	
VITAL, PIERRE M	
ART UNIT	**PAPER NUMBER**
2188	8

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,671	O'CONNOR, DENNIS M.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-16,18-26 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-16,18-26 and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 4, 2004 has been entered.

Response to Amendment

2. This Office Action is in response to applicant's communication filed March 4, 2004 in response to PTO Office Action mailed February 18, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

3. Claims 1-30 have been presented for examination in this application. In response to the last Office Action, claims 1, 11, 21 and 22 have been amended. Claims 7, 17 and 27 have been canceled. No claims have been added. As a result, claims 1-6,8-16,18-26 and 28-30 are now pending in this application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 5, 6, 8, 11, 12, 15, 16,18, 21, 22, 25, 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,463,507) and Cheriton (US5,893,155).

As per claim 1, Arimilli discloses a method comprising defining a multilevel cache [*e.g., L1 and L2*; col. 8, lines 19-21] including a core having relatively faster components [*L1 cache is faster since it is closest to processor core*; col. 8, lines 19-21; col. 9, lines 47-50]; and a region including relatively slower components [*directory of the lower level (L2) cache, L2 cache is slower than L1 cache*; col. 5, line 32; *L1 cache is composed of high-speed components, L2 cache can store a much larger amount of information and encounters a longer access penalty than the L1 cache*; col. 2, lines 34-46]; and managing the core from said region [*upper level cache in the core is updated by searching lower level cache directory*; col. 5, lines 30-33].

However, Arimilli does not specifically teach performing virtual to physical translation in said region as recited in the claim.

Cheriton discloses performing virtual to physical translation in a slower region of cache memory to allow writeback of a virtually addressed cache (col. 15, lines 4-11). Since the technology for implementing virtual to physical translation in a slower region of cache memory was well know and since performing virtual to physical translation in a

slower region of cache memory to allow writeback of a virtually addressed cache, an artisan in the art would have been motivated to implement virtual to physical translation in a slower region of cache memory in the system of Arimilli. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use virtual to physical translation in a slower region of cache memory because it was well known to benefit by allowing writeback of a virtually addressed cache.

As per claim 2, Arimilli discloses managing the core from a level 2 cache [*upper level cache in the core is updated by searching lower level (L2) cache directory*; col. 5, lines 30-33].

As per claim 5, Arimilli discloses using a write-through core cache [*L1 cache may be a store-through cache*; col. 10, lines 62-63].

As per claim 6, Arimilli discloses implementing a line replacement policy in said region [*L2 controller 214 controls L1 least recently used (LRU) unit and maintains an hybrid L2 LRU 232*; Fig. 4; col. 10, lines 20-30].

As per claim 8, Arimilli discloses handling a core cache miss by passing the details of the access to said region [*if load operation in L1 results in a miss, the load address is piped out to lower level storage (L2) subsystem*; col. 8, lines 43-49].

As per claim 11, Arimilli discloses an article comprising a medium storing instructions [*L1 instruction cache 254*; Fig. 5] that enable a processor based system to define a multilevel cache [*e.g., L1 and L2*; col. 8, lines 19-21] including a core having relatively faster components [*L1 cache is faster since it is closest to processor core*; col. 8, lines

19-21; col. 9, lines 47-50; *L1 cache is composed of high-speed components;* col. 2, lines 34-46]; and a region including relatively slower components [*directory of the lower level (L2) cache, L2 cache is slower than L1 cache*; col. 5, line 32; *L2 cache can store a much larger amount of information and encounters a longer access penalty than the L1 cache*; col. 2, lines 34-46]; and managing the core from said region [*upper level cache in the core is updated by searching lower level cache directory*; col. 5, lines 30-33].

However, Arimilli does not specifically teach performing virtual to physical translation in said region as recited in the claim.

Cheriton discloses performing virtual to physical translation in a slower region of cache memory to allow writeback of a virtually addressed cache (col. 15, lines 4-11). Since the technology for implementing virtual to physical translation in a slower region of cache memory was well know and since performing virtual to physical translation in a slower region of cache memory to allow writeback of a virtually addressed cache, an artisan in the art would have been motivated to implement virtual to physical translation in a slower region of cache memory in the system of Arimilli. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use virtual to physical translation in a slower region of cache memory because it was well known to benefit by allowing writeback of a virtually addressed cache.

As per claim 12, Arimilli discloses managing the core from a level 2 cache [*upper level cache in the core is updated by searching lower level (L2) cache directory*; col. 5, lines 30-33].

As per claim 15, Arimilli discloses using a write-through core cache [*L1 cache may be a store-through cache*; col. 10, lines 62-63].

As per claim 16, Arimilli discloses implementing a line replacement policy in said region [*L2 controller 214 controls L1 least recently used (LRU) unit and maintains an hybrid L2 LRU 232*; Fig. 4; col. 10, lines 20-30].

As per claim 18, Arimilli discloses handling a core cache miss by passing the details of the access to said region [*if load operation in L1 results in a miss, the load address is piped out to lower level storage (L2) subsystem*; col. 8, lines 43-49].

As per claim 21, Arimilli discloses a processor [*CPU 150*; Fig. 3]; a multilevel cache [*e.g., L1 and L2*; col. 8, lines 19-21] including a core having relatively faster components [*L1 cache is faster since it is closest to processor core*; col. 8, lines 19-21; col. 9, lines 47-50]; and a region including relatively slower components [*directory of the lower level (L2) cache, L2 cache is slower than L1 cache*; col. 5, line 32]; and a storage coupled to said processor storing instructions [*L1 instruction cache 254*; Fig. 5] that enable the processor to manage the core from said region [*upper level cache in the core is updated by searching lower level cache directory*; col. 5, lines 30-33].

However, Arimilli does not specifically teach performing virtual to physical translation in said region as recited in the claim.

Cheriton discloses performing virtual to physical translation in a slower region of cache memory to allow writeback of a virtually addressed cache (col. 15, lines 4-11). Since the technology for implementing virtual to physical translation in a slower region

of cache memory was well know and since performing virtual to physical translation in a slower region of cache memory to allow writeback of a virtually addressed cache, an artisan in the art would have been motivated to implement virtual to physical translation in a slower region of cache memory in the system of Arimilli. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use virtual to physical translation in a slower region of cache memory because it was well known to benefit by allowing writeback of a virtually addressed cache.

As per claim 22, Arimilli discloses managing the core from a level 2 cache [*upper level cache in the core is updated by searching lower level (L2) cache directory*; col. 5, lines 30-33].

As per claim 25, Arimilli discloses using a write-through core cache [*L1 cache may be a store-through cache*; col. 10, lines 62-63].

As per claim 26, Arimilli discloses implementing a line replacement policy in said region [*L2 controller 214 controls L1 least recently used (LRU) unit and maintains an hybrid L2 LRU 232*; Fig. 4; col. 10, lines 20-30].

As per claim 28, Arimilli discloses handling a core cache miss by passing the details of the access to said region [*if load operation in L1 results in a miss, the load address is piped out to lower level storage (L2) subsystem*; col. 8, lines 43-49].

6. Claims 3, 4, 9-10, 13, 14, 19-20, 23, 24 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,463,507) and Cheriton (US5,893,155) and Wu (US5,668,968).

As per claims 3, 13 and 23, the combination of Arimilli and Cheriton discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Arimilli and Cheriton does not specifically teach using a virtual address to index the core to avoid the need for an address translation mechanism as recited in the claims.

Wu discloses using a virtual address to index the core to avoid the need for an address translation mechanism [*portion of the virtual address is used to index the L1 cache, and L1 cache uses a real pointer to point to the corresponding line in L2 cache*; col. 6, lines 52-56; lines 66-67].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Cheriton and Wu before him at the time the invention was made, to modify the system of Arimilli and Cheriton to include using a virtual address to index the core to avoid the need for an address translation mechanism because it would have (1) reduced the cache coherence complexity in the system because the real, lower level cache always include the lines in the virtual, upper level cache [col. 6, lines 40-45] and (2) modified the L1 cache with limited overhead because the needed information can be quickly accessed [col. 6, lines 49-51] as taught by Wu.

As per claims 4, 14 and 24, the combination of Arimilli and Cheriton discloses the claimed invention as detailed above in the previous paragraphs. Arimilli further discloses placing functions relating to valid bits in the core [*one state bit, valid/invalid is provided*; col. 10, lines 61-64]. However, the combination of Arimilli and Cheriton does not specifically teach placing functions relating to tags and valid bits as well as the data itself in the core as recited in the claims.

Wu discloses placing functions relating to tags as well as the data itself in the core [*the remainder of the virtual address becomes a virtual address tag stored in L1 cache directory to indicate whether the corresponding line of data is stored in L1*; col. 6, line 51 – col. 7, line 3].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Cheriton and Wu before him at the time the invention was made, to modify the system of Arimilli and Cheriton to include placing functions relating to tags as well as the data itself in the core; because it would have (1) reduced the cache coherence complexity in the system because the real, lower level cache always include the lines in the virtual, upper level cache [col. 6, lines 40-45] and (2) modified the L1 cache with limited overhead because the needed information can be quickly accessed [col. 6, lines 49-51] as taught by Wu.

As per claims 9, 19 and 29, the combination of Arimilli and Cheriton discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Arimilli and Cheriton does not specifically teach enabling said region to

use a memory translation mechanism to determine the physical address and attributes of the access as recited in the claims.

Wu discloses enabling said region to use a memory translation mechanism to determine the physical address and attributes of the access [*TLB generates real address which comprises a 20-bit real page number and a 12-bit offset*; col. 10, lines 39-43].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Cheriton and Wu before him at the time the invention was made, to modify the system of Arimilli and Cheriton to include enabling said region to use a memory translation mechanism to determine the physical address and attributes of the access because it would have (1) reduced the cache coherence complexity in the system because the real, lower level cache always include the lines in the virtual, upper level cache [col. 6, lines 40-45] and (2) modified the L1 cache with limited overhead because the needed information can be quickly accessed [col. 6, lines 49-51] as taught by Wu.

As per claims 10, 20 and 30, the combination of Arimilli and Cheriton discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Arimilli and Cheriton does not specifically teach checking to see if the requested data is in a storage associated with said region as recited in the claims.

Wu discloses checking to see if the requested data is in a storage associated with said region [*the remainder of the real address indicates whether the corresponding line of data is stored in L2 cache*; col. 7, lines 4-8].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Cheriton and Wu before him at the time the invention was made, to modify the system of Arimilli and Cheriton to include checking to see if the requested data is in a storage associated with said region because it would have (1) reduced the cache coherence complexity in the system because the real, lower level cache always include the lines in the virtual, upper level cache [col. 6, lines 40-45] and (2) modified the L1 cache with limited overhead because the needed information can be quickly accessed [col. 6, lines 49-51] as taught by Wu.

Response to Arguments

7. Applicant's arguments with respect to claims 1-6, 8-16, 18-26 and 28-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-

5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre M. Vital
Art Unit 2188
March 14, 2004